IN THE CLAIMS:

Please amends Claim 1 and 12 as shown in this complete set of all pending Claims:

1. (Currently amended) An equalizer for use in a communication device, comprising:

a sampler that samples a signal indicative of an input communication signal to determine digital decision output signals having a predetermined data rate;

a filter that receives digital decision output signals from said sampler and generates equalization signals therefrom; and

a summer coupled to the sampler and the filter, said summer combines together the input communication signal with the equalization signals;

wherein a plurality of clocks control timing associated with the sampler, said clocks having frequencies that are less than a data rate of the communication device;

wherein the equalizer includes a sensitivity test process in which the at-speed sensitivity of the equalizer can be determined, the process includes disabling an input amplifier, providing a predetermined set of tap coefficients to the filter, determining if the sampler generates a repeating pattern associated with the set of tap coefficients, and repeating the sensitivity test process with other predetermined sets of tap coefficients until the sampler no longer determines the repeating pattern associated the set of tap coefficients provided to the filter.

2. (Original) The equalizer of claim 1 wherein said clocks have frequencies that are one-half the predetermined data rate.

3. (Original) The equalizer of claim 1 wherein said clocks include two clocks that are 180 degrees out of phase with respect to each other and activate the sampler on rising edges of the two clocks.

4. (Original) The equalizer of claim 1 wherein said plurality of clocks comprise a set of quadrature clocks.

5. (Original) The equalizer of claim 4 further comprising a clock circuit coupled to said filter and said sampler, said clock circuit generates a plurality of inter-symbol interference ("ISI") cancellation clock signals that operate said filter from the set of quadrature clocks used to operate the sampler.

6. (Canceled)

7. (Original) The equalizer of claim 1 wherein the filter receives unlatched digital decision output signals from said sampler.

8. (Original) The equalizer of claim 1 wherein said sampler comprises a pair of processing paths, one path for generating gradient bits and another path for generating data bits, each path comprising an amplifier and at least one sense amplifier.

9. (Original) The equalizer of claim 1 wherein the equalization signals comprise inter-symbol interference ("ISI") equalization currents and the equalizer further comprises an input amplifier coupled to the summer and having a gain and the equalizer also comprises a coefficient normalization circuit that normalizes the ISI equalization currents to the input amplifier's gain.

10. (Original) The equalizer of claim 1 wherein the filter comprises one or more taps, the sampler comprises one or more sense amplifiers, and wherein equalization can be disabled in the equalizer while preserving currents from the one or more taps by forcing the one or more sense amplifiers into a pre-charge state.

11. (Original) The equalizer of claim 10 wherein equalization can be enabled by releasing the one or more sense amplifiers from the pre-charge state.

12. (Currently amended) An equalizer, comprising:

a sampler that samples a signal indicative of an input communication signal to determine digital decision output signals;

a filter that receives digital decision output signals from said sampler and generates equalization signals therefrom;

a summer coupled to the sampler and the filter, said summer combines together the input communication signal with the equalization signals; and

a clock circuit coupled to said filter and said sampler, said clock circuit generates a plurality of inter-symbol interference ("ISI") cancellation clock signals that operate said filter from a set of quadrature clocks used to operate the sampler;

wherein the equalizer includes a sensitivity test process in which the at-speed sensitivity of the equalizer can be determined, the process includes disabling an input amplifier, providing a predetermined set of tap coefficients to the filter, determining if the sampler generates a repeating pattern associated with the set of tap coefficients, and repeating the sensitivity test process with other predetermined sets of tap coefficients until the sampler no longer determines the repeating pattern associated the set of tap coefficients provided to the filter.

13. (Original) The equalizer of claim 12 wherein the clock circuit comprises variable time delay elements whose time delay can be set during a calibration of the ISI cancellation clocks.

14. (Previously presented) The equalizer of claim 12 wherein said quadrature clocks have frequencies that are less than a data rate of said digital decision output signals.

15. (Canceled)

16. (Original) The equalizer of claim 12 wherein the filter receives unlatched digital decision output signals from said sampler.

17. (Original) The equalizer of claim 12 wherein said sampler comprises a pair of processing paths, one path for generating gradient bits and another path for generating data bits, each path comprising an amplifier and at least one sense amplifier.

18. (Original) The equalizer of claim 12 wherein the equalization signals comprise inter-symbol interference ("ISI") equalization currents and the equalizer further comprises an input amplifier coupled to the summer and having a gain and the equalizer also comprises a coefficient normalization circuit that normalizes the ISI equalization currents to the input amplifier's gain.

19. (Original) The equalizer of claim 12 wherein the filter comprises one or more taps, the sampler comprises one or more sense amplifiers, and wherein equalization can be disabled in the equalizer while preserving currents from the one or more taps by forcing the one or more sense amplifiers into a pre-charge state.

20. (Original) An equalizer, comprising:

an input amplifier that receives an input communication signal;

a sampler that samples a signal indicative of an input communication signal to generate digital decision output signals;

a filter that receives digital decision output signals from said sampler and generates equalization signals therefrom;

a summer coupled to the sampler and the filter, said summer combines together the input communication signal with the equalization signals; and

wherein the equalizer includes a sensitivity test process in which the at-speed sensitivity of the equalizer can be determined, the process includes disabling the input amplifier, providing a predetermined set of tap coefficients to the filter, determining if the sampler generates a repeating pattern associated with the set of tap coefficients, and repeating the sensitivity test process with other predetermined sets of tap coefficients until the sampler no longer determines the repeating pattern associated the set of tap coefficients provided to the filter.

21. (Original) The equalizer of claim 20 wherein the sets of tap coefficients are provided to the filter in order from a maximum value to a minimum value of the tap coefficients.

22. (Original) The equalizer of claim 20 wherein the filter receives unlatched digital decision output signals from said sampler.

23. (Original) The equalizer of claim 20 wherein said sampler comprises a pair of processing paths, one path for generating gradient bits and another path for generating data bits, each path comprising an amplifier and at least one sense amplifier.

24. (Original) The equalizer of claim 20 wherein the equalization signals comprise inter-symbol interference ("ISI") equalization currents and the equalizer further comprises an input amplifier coupled to the summer and having a gain and the equalizer also comprises a coefficient normalization circuit that normalizes the ISI equalization currents to the input amplifier's gain.

25. (Original) The equalizer of claim 20 wherein the filter comprises one or more taps, the sampler comprises one or more sense amplifiers, and wherein equalization can be disabled in the equalizer while preserving currents from the one or more taps by forcing the one or more sense amplifiers into a pre-charge state.

26-31. (Canceled)